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SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. BOX 2938
MINNEAPOLIS, MN 55402

EXAMINER	
KIM, HONG CHONG	

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BEFORE THE BOARD OF PATENT APPEALS

AND INTERFERENCES

Paper No. 32

Application Number: 08/984,562

Filing Date: 12/03/97

Appellant(s): Mailloux et al.

Timothy B. Clise

For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 2/10/2003.

(1) Real Party in Interest

A statement identifying the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

A statement identifying the related appeals and interferences which will directly affect or be directly affected by or have a bearing on the decision in the pending appeal is contained in the brief.

(3) Status of Claims

The statement of the status of the claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Invention

The summary of invention contained in the brief is correct.

(6) Issues

The appellant's statement of the issues in the brief is correct.

(7) Grouping of Claims

The appellant's statement in the brief that all claims are to be taken independently of each other and each stands alone for the purpose of this appeal is not agreed with because Applicant has not provided independent argument for each of the claims that allegedly stand alone for the purposes of this appeal, see 37 CFR 1.192(c)(7)(8) and MPEP § 1206. Applicant provides nine arguments that seemingly apply to all of the claims, therefore, the Examiner believes that grouping of claims into nine groups is appropriate:

Group I, claims 22, 59, & 66, a mode select circuitry for switching between a burst mode and a pipelined mode of operation;

Group II, claims 23, 24, 67, & 68, external mode select;

Group III, claims 25, 69, & 70, write enable and output enable;

Group IV, claim 28, using a second external address subsequent to a first external address;

Group V, claims 29 & 72, EDO;

Group VI, claims 30 & 31, any type of address strobe latency in conjunction with pipelined mode operation;

Group VII, claim 61, a multiplexer and internal mode;

Group VIII, claims 26, 27, & 71, counter; and

Group IX, claim 32, asynchronously-accessible dynamic RAM;

Merely pointing out differences in what the claim cover is not an argument as to why the claims are separately patentable.

(8) Claims Appealed

The copy of the appealed claims contained in the Appendix to the brief is correct.

(9) Prior Art of Record

The following is a listing of the prior art of record relied upon in the rejection of claims under appeal.

5,610,864	Manning	3-1997
5,729,503	Manning	3-1998

(10) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claims 22-32, 59, 61 & 66-72 are rejected under 35 U.S.C. 102(e). This rejection is set forth in prior Office Action, Paper No. 29.

Claims 22-32, 59, 61 & 66-72 are rejected under 35 U.S.C. 103 (a). This rejection is set forth in prior Office Action, Paper No. 29.

(11) Response to Argument

Applicant's arguments fail to comply with 37 CFR 1.111(b) because they amount to a general allegation that the claims define a patentable invention without specifically pointing out how the language of the claims patentably distinguishes them from the references.

In response to applicant's argument that there is no suggestion to combine the references (bottom of page 5 and top of page 10), the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, Manning (864) discloses a pipelined mode (col. 5 lines 43-50) for the purpose of increasing the throughput by accessing data per every cycle (col 5 lines 46-48) thereby increasing the system throughput.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify a standard EDO page mode of 503 with a pipelined mode of 864 because it would increase the throughput by accessing data per every cycle thereby increasing the system throughput.

In response to applicant's argument at the center of page 10 in the Appeal Brief that the cited references do not disclose "selecting or switching between a burst mode and a pipelined mode" has been fully considered but it is not persuasive.

Manning (864) discloses selecting or switching between a burst mode and a pipelined mode. "The current invention include a pipelined architecture where memory accesses are performed sequentially" (col. 5 lines 43-49 in Manning) and "switching between burst EDO mode and standard EDO mode" (see col 6 lines 14-16 & Fig. 1 and col. 7 lines 44-55 in Manning) read on this limitation. In other words, in order to work in a standard EDO memory including a pipelined architecture, one has to select a pipelined mode if one is in a burst mode. Also it is well known in the memory art that the pipelined memory architecture provides speed advantages by enabling more than one memory read, memory write, memory address input, memory data input or memory data output to be processed simultaneously. In other words, the pipelined architecture advantage in a memory effectively hides memory wait state, specifically this is accomplished by overlapping memory operations using a pipe. Another advantage that the pipelined memory architecture has over the parallel read and write architecture is a reduction in required circuitry. In particular, the parallel architecture requires two sample-and-hold circuits (one in each buffer) per read or write circuit. The pipelined architecture requires only a single sample-and-hold circuit per read or write circuit. Thus, the pipelined architecture can reduce circuit cost by decreasing the required integrated circuit area. Therefore, given the teachings of above reference one of the ordinary skill in the art at the time the invention was made would have been lead to an obvious

fashion to provide a pipelined EDO mode circuitry since Manning (864) discloses that the current invention include a pipelined architecture (col. 5 lines 43-49) which would increase accessing speed.

In response to applicant's argument at the center of page 12 in the Appeal Brief that the cited references do not disclose "asynchrous EDO" has been fully considered but it is not persuasive

Manning (503) discloses the standard EDO (col. 1 line 31 and Fig. 1) which constitutes asynchronous memory, since the standard EDO does not require a clock, Manning also discloses a functional description of the SDRAM (col. 1 lines 42-58) in the background section. Synchronous operation mention in the 503 reference is synchronous burst address generation in response to the CAS transition although an initial external address is inputted in asynchronously (col. 3 lines 5-10).

Manning (864) also discloses the standard EDO (col. 6 lines 14-16) which constitutes asynchronous memory operation, since the standard EDO does not require a clock or strobe signal, see Fig. 1.

In response to applicant's argument at the top of page 11 in the Appeal Brief that only a burst EDO memory includes pipelined architecture has been fully considered but it is not persuasive.

Examiner disagrees with applicants because Manning discloses that "The current invention include a pipelined architecture where memory accesses are performed sequentially", col 5 lines 43-49. In other words, pipelined architecture can be used on standard EDO, fast page mode, static column, and burst modes (see col. 7 lines 50-54), therefore, in order to work in a standard EDO memory includes pipelined architecture, one has to select a pipelined mode.

A. Response to Argument of Claim Group I, (claims 22, 59, & 66)

1. Appellants' argument at the bottom of page 7 and the top of page 8 in the Appeal Brief that the cited references do not disclose "providing or receiving a mode control signal, or circuitry for switching or selecting between a burst mode and a pipelined mode" has been fully considered but it is not persuasive.

Manning (864) discloses providing or receiving a mode control signal, or circuitry (col. 6 lines 14+ and col. 7 lines 44-54) for switching or selecting between a burst mode and a pipelined mode. "The current invention include a pipelined architecture where memory accesses are performed sequentially" (col. 5 lines 43-49 in Manning) and "switching between burst EDO mode and standard EDO mode" (see col 6 lines 14-16 & Fig. 1 and col. 7 lines 44-55 in Manning) read on this limitation. In other words, in order to work in a standard EDO memory including a pipelined architecture, one has to select a pipelined mode if one is in a burst mode. Also it is well known in the memory art that the pipelined memory architecture provides speed advantages by enabling more than one memory read, memory write, memory address input, memory data input

or memory data output to be processed simultaneously. In other words, the pipelined architecture advantage in a memory effectively hides memory wait state, specifically this is accomplished by overlapping memory operations using a pipe. Another advantage that the pipelined memory architecture has over the parallel read and write architecture is a reduction in required circuitry. In particular, the parallel architecture requires two sample-and-hold circuits (one in each buffer) per read or write circuit. The pipelined architecture requires only a single sample-and-hold circuit per read or write circuit. Thus, the pipelined architecture can reduce circuit cost by decreasing the required integrated circuit area. Therefore, Manning (864) discloses providing or receiving a mode control signal, or circuitry for switching or selecting between a burst mode and a pipelined mode (col. 6 lines 14+, col. 7 lines 44-54, col. 5 lines 43-49, and col 6 lines 14-16 & Fig. 1).

B. Response to Argument of Claim Group II, (claims 23, 24, 67 & 68)

1. Appellants' argument at the top of page 8 in the Appeal Brief that the cited references do not disclose "an external mode select signal" has been fully considered but it is not persuasive.

Manning (864) discloses an external mode select signal (col. 6 lines 14+ and col. 7 lines 44-54 and Fig. 1).

C. Response to Argument of Claim Group III, (claims 25, 69, & 70)

1. Appellants' argument at the center of page 8 in the Appeal Brief that the cited references do not disclose "using write enable and a separate output enable signal for determining the mode control signal" has been fully considered but it is not persuasive.

Manning (864) discloses using write enable and a separate output enable signal for determining the mode control signal (col. 7 lines 44-54, specifically, line 54) .

D. Response to Argument of Claim Group IV, (claim 28)

1. Appellants' argument at the center of page 8 in the Appeal Brief that the cited references do not disclose "using a second external address subsequent to a first external address" has been fully considered but it is not persuasive.

Manning (864) discloses using a second external address subsequent to a first external address. "The current invention include a pipelined architecture where memory accesses are performed sequentially --- In a pipelined architecture the overall throughput of the memory approaches one access per cycle" (col. 5 lines 43-49 in Manning) reads on this limitation since the second address should be provided subsequent to the first address in a pipelined mode operation. In other words, accessing a non burst memory such as a standard EDO memory including a pipelined architecture, a new external address should be provided to an input address terminal every memory access cycle in order to take an advantage of the pipelined architecture since the pipelined architecture effectively hides memory wait state, specifically this is accomplished by overlapping memory operations using a pipe.

E. Response to Argument of Claim Group V, (claims 29 & 72)

1. Appellants' argument at the bottom of page 8 in the Appeal Brief that the cited references do not disclose "the pipelined mode disclosed as being an EDO mode" has been fully considered but it is not persuasive.

Manning (864) discloses the pipelined mode disclosed as being an EDO mode. "The current invention include a pipelined architecture where memory accesses are performed sequentially" (col. 5 lines 43-49 in Manning) and "switching between burst EDO mode and standard EDO mode" (see col 6 lines 14-16 & Fig. 1 and col. 7 lines 44-55 in Manning) read on this limitation.

F. Response to Argument of Claim Group VI, (claims 30 & 31)

1. Appellants' argument at the bottom of page 8 in the Appeal Brief that the cited references do not disclose "any type of address strobe latency in conjunction with a pipelined mode operation" has been fully considered but it is not persuasive.

Manning (864) discloses any type of address strobe latency in conjunction with a pipelined mode operation. "The data out of the memory is offset by a number of cycles equal to the pipeline length and /or the desired latency from/CAS" (col. 5 lines 43-49 in Manning) reads on this limitation.

G. Response to Argument of Claim Group VII, (claim 61)

1. Appellants' argument at the bottom of page 8 in the Appeal Brief that the cited references do not disclose "a multiplexer coupled to -- control logic for receiving-- the internal mode control signal" has been fully considered but it is not persuasive.

Manning (864) discloses a multiplexer coupled to -- control logic for receiving the first external address (Fig. 1 Ref. 26, controlling the column address counter/latch between burst and pipelined modes reads on this limitation, because during the burst operation, the address is incremented internal to the device eliminating the need for external address lines to switch at high frequencies, col. 3 lines 19-21 and col. 5 lines 50-57, however, during the pipelined operation, each column address is provided one access per cycle, col. 5 line 43-50. In other words, during the burst mode, an internal counter/latch path is selected however, during the pipelined mode, an external counter/latch path is selected, see also col. 6 lines 26-34)-- the internal mode control signal (a line to Ref. 26 from Refs. 38 and 40 in Fig. 1).

H. Response to Argument of Claim Group VIII, (claims 26, 27, & 71)

Manning (864) discloses a counter (Fig. 1 Ref. 26).

I. Response to Argument of Claim Group IX, (claim 32)

Manning (864) discloses asynchrously accessible random access memory (the standard EDO constitutes asynchronous memory, col. 6 lines 14-16, since the standard EDO does not require a clock or strobe signal, see Fig. 1).

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Hong Kim
May 28, 2003

Conferees

Hiep Nguyen
PE

Matt Kim
SPE

Timothy B Clise
SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. BOX 2938
MINNEAPOLIS, MN, 55402